



1 Block Diagram

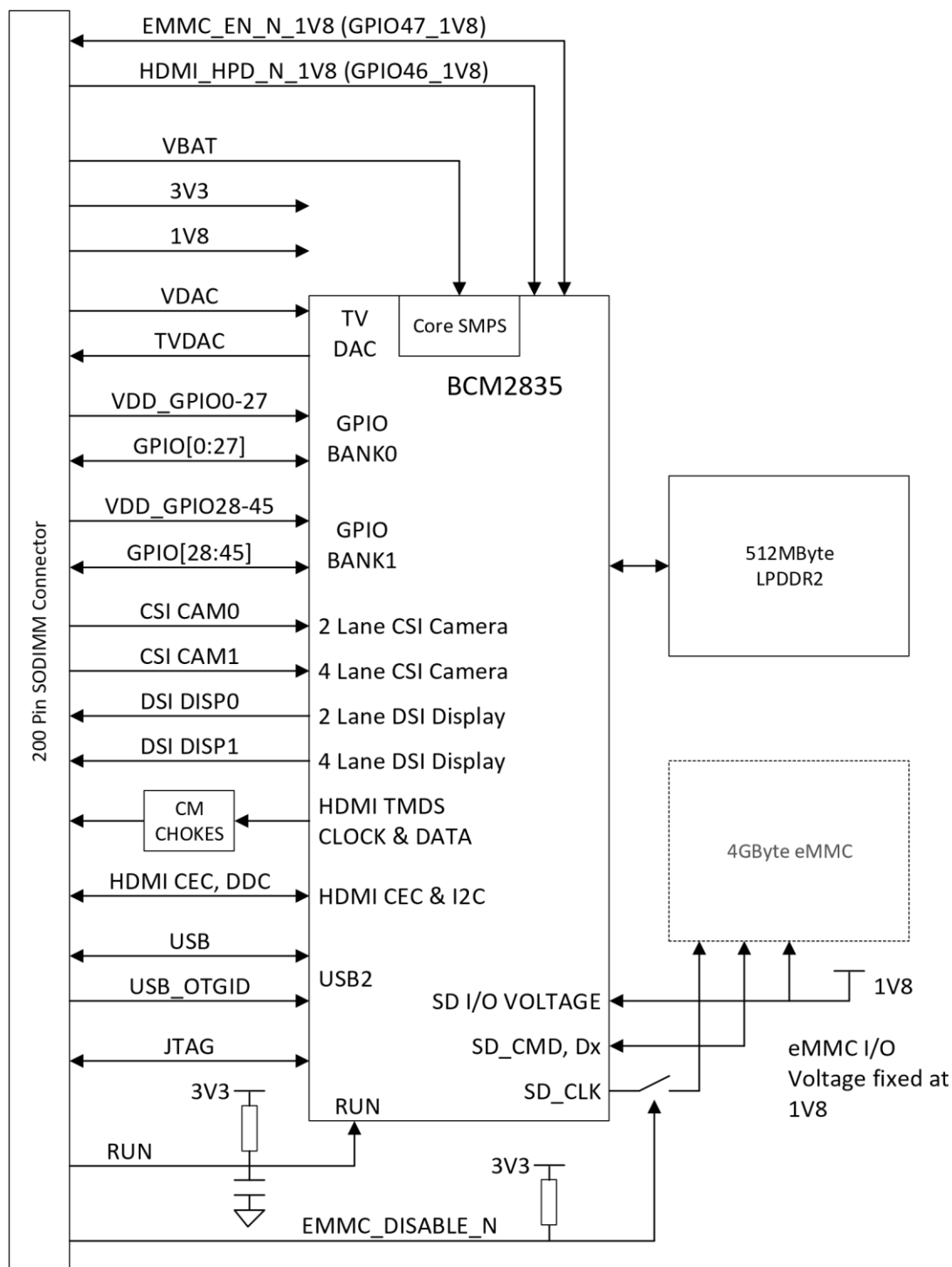


Figure 1: CM1 Block Diagram

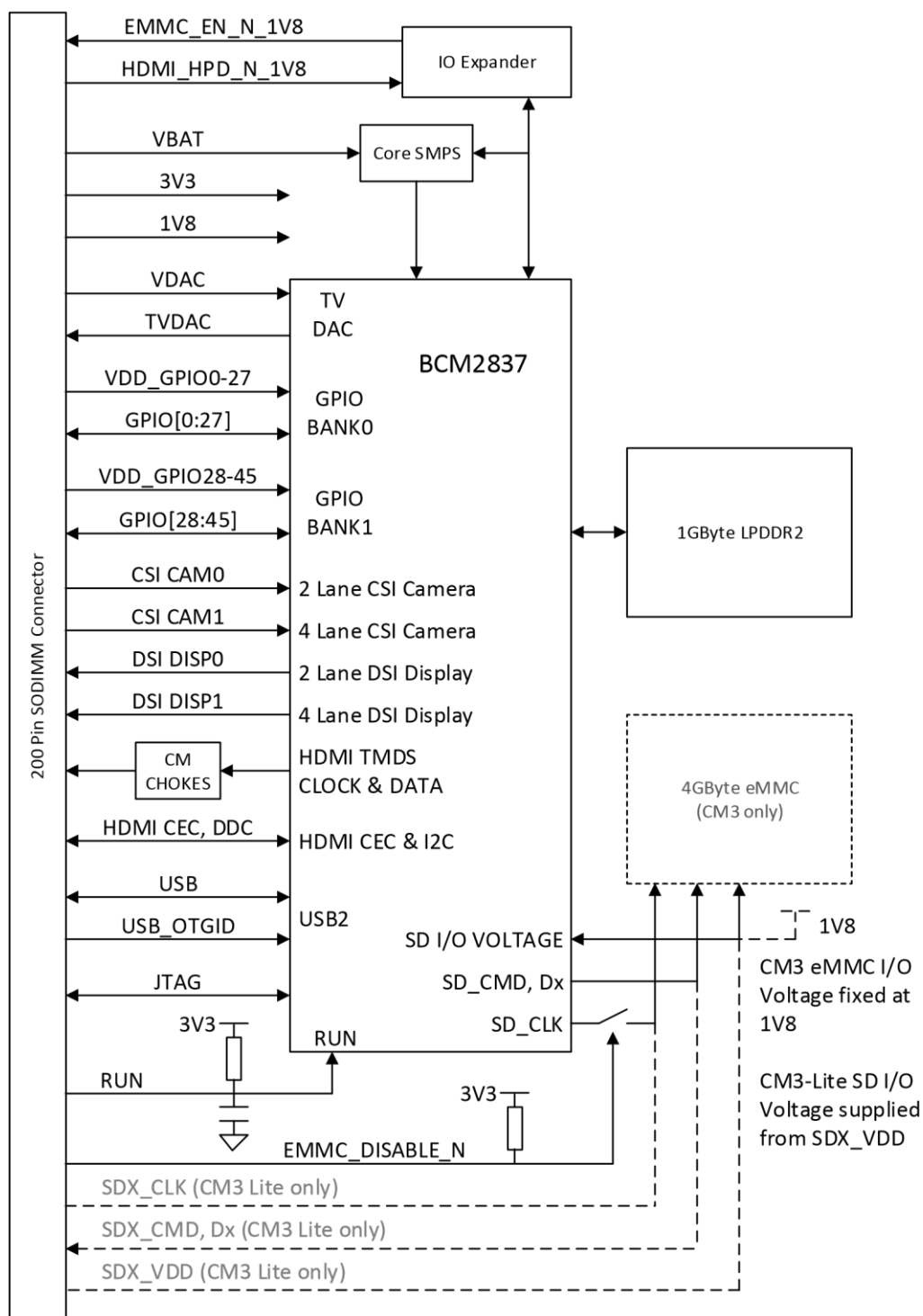


Figure 2: CM3/CM3L Block Diagram



2 Mechanical Specification

The Compute Modules conform to JEDEC MO-224 mechanical specification for 200 pin DDR2 (1.8V) SODIMM modules (with the exception that the CM3, CM3L modules are 31mm in height rather than 30mm of CM1) and therefore should work with the many DDR2 SODIMM sockets available on the market. (Please note that the pinout of the Compute Module is not the same as a DDR2 SODIMM module; they are not electrically compatible.)

The SODIMM form factor was chosen as a way to provide the 200 pin connections using a standard, readily available and low cost connector compatible with low cost PCB manufacture.

The maximum component height on the underside of the Compute Module is 1.2mm.

The maximum component height on the top side of the Compute Module is 1.5mm.

The Compute Module PCB thickness is 1.0mm +/- 0.1mm.

Note that the location and arrangement of components on the Compute Module may change slightly over time due to revisions for cost and manufacturing considerations; however, maximum component heights and PCB thickness will be kept as specified.

Figure 3 gives the CM1 mechanical dimensions. Figure 4 gives the CM3 and CM3L mechanical dimensions.

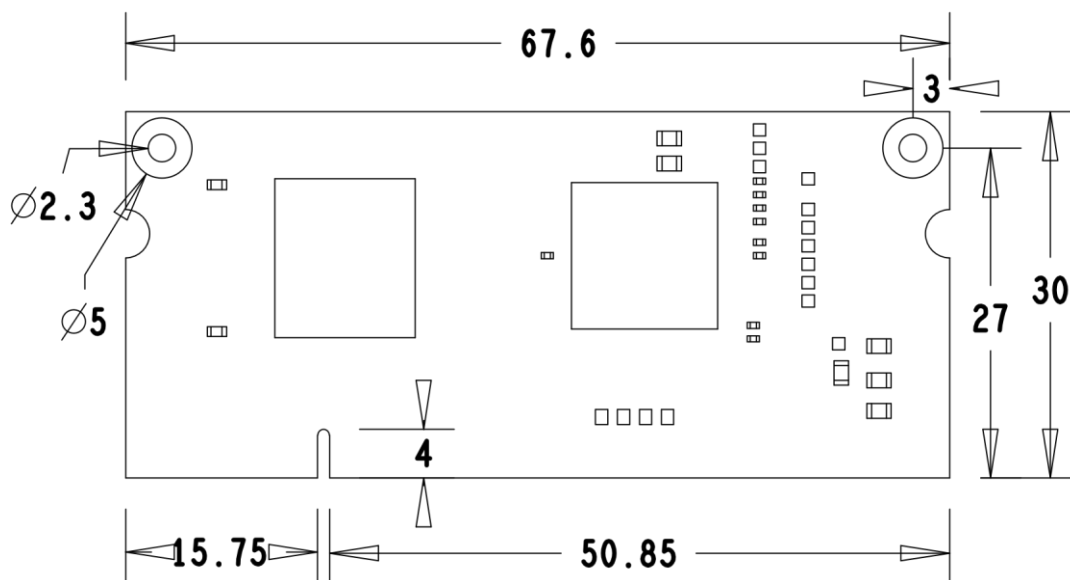


Figure 3: CM1 Mechanical Dimensions

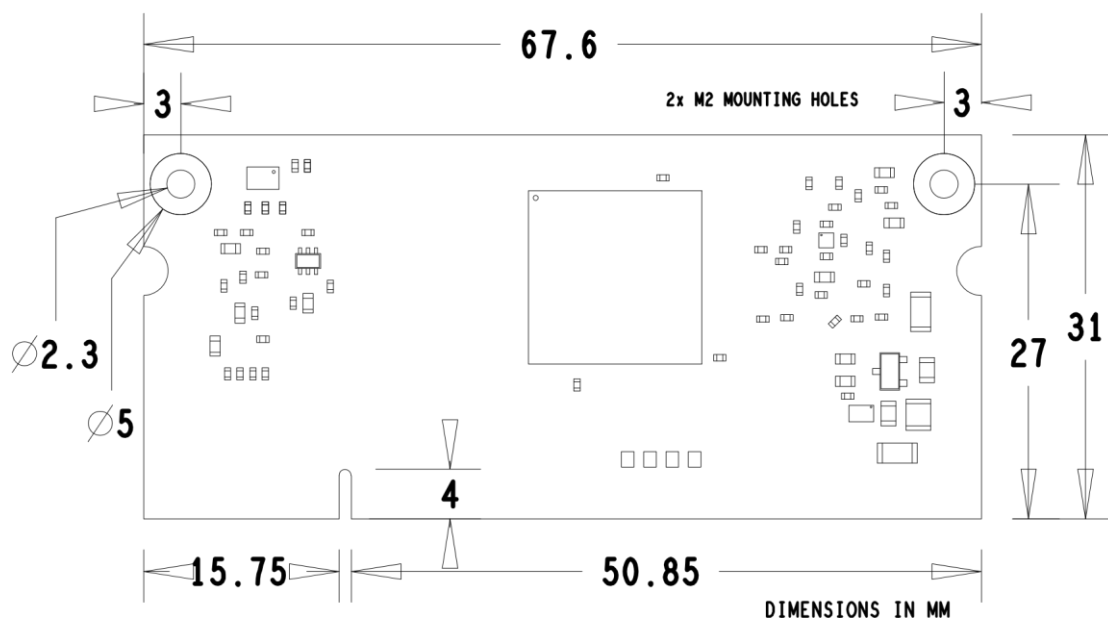


Figure 4: CM3 and CM3L Mechanical Dimensions

3 Pin Assignments

CM1	CM3-Lite	CM3	PIN	PIN	CM3	CM3-Lite	CM1
GND			1	2		HMC_DISABLE	N
GPIO0			3	4	NC	SDX_VDD	NC
GPIO1			5	6	NC	SDX_VDD0	NC
GND			7	8	G_VD		NC
GPIO2			9	10	NC	SDX_CLK	NC
GPIO3			11	12		SDX_CMD0	NC
GND			13	14	G_VD		NC
GPIO4			15	16	NC	SDX_D0	NC
GPIO5			17	18	NC	SDX_D1	NC
GND			19	20	G_VD		NC
GPIO6			21	22		SDX_D2	NC
GPIO7			23	24	NC	SDX_D3	NC
GND			25	26	GND		
GPIO8			27	28	GPIO28		
GPIO9			29	30	GPIO29		
GND			31	32		GND	
GPIO10			33	34		GPIO30	
GPIO11			35	36		GPIO31	
GND			37	38		GND	
GPIO27_VDD			39	40		GPIO27_VDD	
GPIO28-45_VDD			41	42		GPIO28-45_VDD	
GND			43	44		GND	
GPIO12			45	46		GPIO32	
GPIO13			47	48		GPIO33	
GND			49	50	GND		
GPIO14			51	52		GPIO34	
GPIO15			53	54		GPIO35	
GND			55	56	GND		
GPIO16			57	58	GPIO36		
GPIO17			59	60	GPIO37		
GND			61	62		GND	
GPIO18			63	64		GPIO38	
GPIO19			65	66		GPIO39	
GND			67	68	GND		
GPIO20			69	70		GPIO40	
GPIO21			71	72		GPIO41	
GND			73	74	GND		
GPIO22			75	76	GPIO42		
GPIO23			77	78	GPIO43		
GND			79	80		GND	
GPIO24			81	82		GPIO44	
GPIO25			83	84		GPIO45	
GND			85	86	GND HDMI_HP0_N_1V8		GPIO46_1V8
GPIO26			87	88			
GPIO27			89	90	EMMC_EN_N_1V8		GPIO47_1V8
GND			91	92		GND	
DSIO_DN1			93	94		DSI1_DP0	
DSIO_DP1			95	96		DSI1_DN0	
GND			97	98		GND	
DSIO_DN0			99	100		DSI1_CP	
DSIO_DP0			101	102		DSI1_CN	
GND			103	104	GND		
DSIO_CN			105	106		DSI1_DP3	
DSIO_CP			107	108		DSI1_DN3	
GND HDMI_CLK_N			109	110		GND	
HDMI_CLK_P			111	112		DSI1_DP2	
			113	114		DSI1_DN2	
GND HDMI_D0_N			115	116		GND	
HDMI_D0_P			117	118		DSI1_DP1	
			119	120		DSI1_DN1	
GND HDMI_D1_N			121	122		GND	
HDMI_D1_P			123	124		NC	
			125	126		NC	
GND HDMI_D2_N			127	128		NC	
			129	130		NC	
HDMI_D2_P			131	132		NC	
GND CAM1_DP3			133	134		GND CAM0_DP0	
CAM1_DN3			135	136			
			137	138		CAM0_DN0	
GND CAM1_DP2			139	140		GND	
CAM1_DN2			141	142		CAM0_CP	
			143	144		CAM0_CN	
GND			145	146		GND CAM0_DP1	
CAM1_CP			147	148			
CAM1_CN			149	150		CAM0_DN1	
GND CAM1_DP1			151	152		GND	
CAM1_DN1			153	154		NC	
			155	156		NC	
GND CAM1_DP0			157	158		NC	
			159	160		NC	
CAM1_DN0			161	162		NC	
GND			163	164		GND	
US8_DP			165	166		TVDAC	
US8_DM			167	168		US8_OTGDI0 GND	
GND			169	170			
HDMI_CEC			171	172		VC_TRST_N	
HDMI_SDA			173	174		VC_TDI	
HDMI_SCL			175	176		VC_TMS	
RUN			177	178		VC_TDO	



VDD_CORE (DO NOT CONNECT)	179	180	VC_TCK
GND	181	182	GND
1V8	183	184	1V8
1V8	185	186	1V8
GND	187	188	GND
VDAC	189	190	VDAC
3V3	191	192	3V3
3V3	193	194	3V3
GND	195	196	GND
VBAT	197	198	VBAT
VBAT	199	200	VBAT

Table 2: Compute Module SODIMM Connector Pinout

Table 2 gives the Compute Module pinout and Table 3 gives the Compute Module pin functions.

Pin Name	DIR	Voltage Ref	PDN ¹ State	If Unused	Description/Notes
<i>RUN and Boot Control (see text for usage guide)</i>					
RUN	I	3V3 ^b	Pull High	Leave open	Has internal 10k pull up
EMMC DISABLE N	I	3V3 ^b	Pull High	Leave open	Has internal 10k pull up
EMMC EN N 1V8	O	1V8	Pull High	Leave open	Has internal 2k2 pull up
<i>GPIO</i>					
GPIO[27:0]	I/O	GPIO0-27 VDD	Pull or Hi-Z ^c	Leave open	GPIO Bank 0
GPIO[45:28]	I/O	GPIO28-45 VDD	Pull or Hi-Z ^c	Leave open	GPIO Bank 1
<i>Primary SD Interface^{d,e}</i>					
SDX-CLK	O	SDX VDD	Pull High	Leave open	Primary SD interface CLK
SDX-CMD	I/O	SDX VDD	Pull High	Leave open	Primary SD interface CMD
SDX-Dx	I/O	SDX VDD	Pull High	Leave open	Primary SD interface DATA
<i>USB Interface</i>					
USB-Dx	I/O	-	Z	Leave open	Serial interface
USB-OTGID	I	3V3		Tie to GND	OTG pin detect
<i>HDMI Interface</i>					
HDMI SCL	I/O	3V3 ^b	Z ^f	Leave open	DDC Clock (5.5V tolerant)
HDMI SDA	I/O	3V3 ^b	Z ^f	Leave open	DDC Data (5.5V tolerant)
HDMI CEC	I/O	3V3	Z	Leave open	CEC (has internal 27k pull up)
HDMI CLKx	O	-	Z	Leave open	HDMI serial clock
HDMI Dx	O	-	Z	Leave open	HDMI serial data
HDMI HPD N 1V8	I	1V8	Pull High	Leave open	HDMI hotplug detect
<i>CAM0 (CSI0) 2-lane Interface</i>					
CAM0 Cx	I	-	Z	Leave open	Serial clock

¹ The PDN column indicates power-down state (when RUN pin LOW) ^b Must be driven by an open-collector driver ^c GPIO have software enabled pulls which keep state over power-down ^d Only available on Lite variants ^e The CM will always try to boot from this interface first ^f Requires external pull-up resistor to 5V as per HDMI spec

Table 3: Pin Functions



CAM0 Dx	I	-	Z	Leave open	Serial data
<i>CAM1 (CSI1) 4-lane Interface</i>					
CAM1 Cx	I	-	Z	Leave open	Serial clock
CAM1 Dx	I	-	Z	Leave open	Serial data
<i>DSI0 (Display 0) 2-lane Interface</i>					
DSI0-Cx	O	-	Z	Leave open	Serial clock
DSI0-Dx	O	-	Z	Leave open	
<i>DSI1 (Display 1) 4-lane Interface</i>					
DSI1-Cx	O	-	Z	Leave open	Serial clock
DSI1-Dx	O	-	Z	Leave open	Serial data
<i>TV Out</i>					
TVDAC	O	-	Z	Leave open	Composite video DAC output
<i>JTAG Interface</i>					
TMS	I	3V3	Z	Leave open	Has internal 50k pull up
TRST_N	I	3V3	Z	Leave open	Has internal 50k pull up
TCK	I	3V3	Z	Leave open	Has internal 50k pull up
TDI	I	3V3	Z	Leave open	Has internal 50k pull up
TDO	O	3V3	O	Leave open	Has internal 50k pull up

4 Electrical Specification

Caution! Stresses above those listed in Table 4 may cause permanent damage to the device. This is a stress rating only; functional operation of the device under these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Minimum	Maximum	Unit
VBAT	Core SMPS Supply	-0.5	6.0	V
3V3	3V3 Supply Voltage	-0.5	4.10	V
1V8	1V8 Supply Voltage	-0.5	2.10	V
VDAC	TV DAC Supply	-0.5	4.10	V
GPI00-27 VDD	GPI00-27 I/O Supply Voltage	-0.5	4.10	V
-	GPI028-27 I/O Supply Voltage	-0.5	4.10	V
	Primary SD/eMMC Supply Voltage	-0.5	4.10	V
GPI028-45 VDD				
SDX VDD				



Table 4: Absolute Maximum Ratings

DC Characteristics are defined in Table 5

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{IL}	Input low voltage ²	VDD IO = 1.8V	-	-	0.6	V
		VDD IO = 2.7V	-	-	0.8	V
V_{IH}	Input high voltage ^a	VDD IO = 1.8V	1.0	-	-	V
AC Characteristics are defined in Table 6 and Fig. 5.						
I_{IL}	Input leakage current	TA = +85° C	-	-	5	μ
V_{OL}	Output low voltage ^b	VDD IO = 1.8V, IOL = -2mA	-	-	0.2	V
		VDD IO = 2.7V, IOL = -2mA	-	-	0.15	V
V_{OH}	Output high voltage ^b	VDD IO = 1.8V, IOH = 2mA	1.6	-	-	V
		VDD IO = 2.7V, IOH = 2mA	2.5	-	-	V
I_{OL}	Output low current ^c	VDD IO = 1.8V, VO = 0.4V	12	-	-	mA
		VDD IO = 2.7V, VO = 0.4V	17	-	-	mA
I_{OH}	Output high current ^c	VDD IO = 1.8V, VO = 1.4V	10	-	-	mA
		VDD IO = 2.7V, VO = 2.3V	16	-	-	mA
R_{PU}	Pullup resistor	-	50	-	65	k Ω
R_{PD}	Pulldown resistor	-	50	-	65	k Ω